Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (original) A circuit arrangement comprising:

a first circuit having an output line and an input line;

a second circuit having an input line for receiving signals from the output line of the first circuit, an output line for transmitting signals to the input line of the first circuit; and

a control circuit for controlling signals transmitted from the second circuit output line to the first circuit input line.

2. (original) The circuit arrangement of claim 1 wherein the control circuit controls signals transmitted from the second circuit output line to the first circuit input line in accordance with signals transmitted at the output line of the first circuit.

3. (original) The circuit arrangement of claim 2 wherein the control circuit inhibits the signals transmitted from the second circuit output line to the first circuit input line when the first circuit is transmitting signals at the output line of the first circuit.

4. (original) The circuit arrangement of claim 2, wherein the control circuit keeps the input line of the first circuit at a high state when the first circuit is transmitting signals at the output line.

5. (original) The circuit arrangement of claim 2 wherein the first circuit is a selected one of Universal Asynchronous Receiver/Transmitter (UART) and Universal Synchronous/Asynchronous Receiver/Transmitter (USART).

6. (original) The circuit arrangement of claim 5, wherein the second circuit is a G-Link circuit.

7. (original) The circuit arrangement of claim 2 wherein the second circuit further comprises a bi-directional line.

8. (original) The circuit arrangement of claim 7, wherein short-circuiting the bi-directional line initiates a demonstration mode.

9. (original) The circuit arrangement of claim 8 wherein the shorting circuiting is a short circuit to ground.

10. (original) The circuit arrangement of claim 1 wherein the first circuit generates an interrupt signal if the first circuit receives the signals transmitted from the second circuit.

11. (original) The circuit arrangement of claim 1, wherein signals transmitted from the first circuit at the output line control an external pager module through the second circuit for connecting to a pager service.

12. (original) The circuit arrangement of claim 1, wherein the second circuit further comprises a second input line for receiving IR signals transmitted from an IR blaster sources, the second circuit transmits at the output line the IR signals for remotely controlling an external device.

13. (original) The circuit arrangement of claim 1, wherein the second circuit provides feedback between the output line of the first circuit and the input line of the first circuit.

14. (original) The circuit arrangement of claim 1 wherein the control circuit controls signals transmitted from the second circuit output line to the first circuit input line according to a mode of operation.

15. (original) A method for controlling communication from a serial interface circuit to a receiver-transmitter circuit in a system under control of a CPU and an operating system, the method comprising the steps of:

detecting a mode of operation of the system;

if the mode is a first mode, allowing the serial interface circuit to transmit signals to the receiver-transmitter circuit; and

if the mode is a second mode, detecting whether the receiver-transmitter circuit is transmitting signals to the serial circuit, if the receiver-transmitter is transmitting, prohibiting the serial interface circuit to transmit signals to the receiver-transmitter.

16. (original) The circuit arrangement of claim 15 wherein the receiver-transmitter circuit is a selected one of Universal Asynchronous Receiver/Transmitter (UART) and Universal Synchronous/Asynchronous Receiver/Transmitter (USART).

17. (original) The circuit arrangement of claim 15, wherein the serial interface circuit is a G-Link circuit.

18. (original) The circuit arrangement of claim 15 wherein the serial interface circuit further comprises a bi-directional line.

19. (original) The circuit arrangement of claim 18, wherein short-circuiting the bi-directional line initiates a demonstration mode.

20. (original) The circuit arrangement of claim 19 wherein the shorting circuiting is a short circuit to ground.